AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-6 (cancelled)

7. (currently amended) A semiconductor device comprising:

a first memory cell ~~having a first MIS transistor, a second MIS transistor, a third MIS transistor and a fourth MIS transistor, which are of an N-channel type~~; and

a second memory cell ~~having a fifth MIS transistor, a sixth MIS transistor, a seventh MIS transistor and an eighth MIS transistor, which are of an N-channel type~~,

wherein each of said first memory cell and said second memory cell includes four N-channel type MIS transistors, and

wherein ~~the~~ a gate-insulating film thickness of ~~said~~ a first MIS transistor of said first memory cell is smaller than that of ~~said fifth~~ a first MIS transistor of said second memory cell.

8. (currently amended) The semiconductor device according to claim 7, further comprising:

~~a ninth MIS transistor in~~ an input/output circuit having an MIS transistor; and

a logic circuit having ~~a tenth~~ an MIS transistor, wherein

the gate-insulating film thickness of said ~~ninth~~ MIS transistor of said input/output circuit is larger than that of said first MIS transistor of said first memory cell, and

the gate-insulating film thickness of said ~~tenth~~ MIS transistor of said logic circuit is smaller than that of said ~~fifth~~ first MIS transistor of said second memory cell.

9. (currently amended) The semiconductor device according to claim 7, further comprising:

an input/output circuit; and

a logic circuit, wherein

the gate-insulating film thickness of ~~the~~ an MIS transistor in said logic circuit is equal to that of said first MIS transistor of said first memory cell,

the gate-insulating film thickness of ~~the~~ a MIS transistor in said input/output circuit is equal to that of said ~~fifth~~ first MIS transistor of said second memory cell,

said first memory cell ~~has a ninth MIS transistor and a tenth MIS transistor, which are of a~~ additionally includes two ~~P~~ P-channel type MIS transistors,

said second memory cell ~~has an eleventh MIS transistor and a twelfth MIS transistor, which are of a~~ additionally

includes two ~~P~~ P-channel type MIS transistors,

the four MIS transistors in each of said first memory cell and said second memory cell are arranged such that the gates of ~~said~~ a third MIS transistor and ~~said~~ a fourth MIS transistor are connected to a wordline, the gate of said first MIS transistor is connected to said fourth MIS transistor, the drain thereof is connected to said third MIS transistor, the gate of ~~said~~ a second MIS transistor is connected to said third MIS transistor, and the drain thereof is connected to said ~~second~~ fourth MIS transistor[[.]]

~~the gates of said seventh MIS transistor and said eighth MIS transistor are connected to a wordline, the gate of said fifth MIS transistor is connected to said eighth MIS transistor, the drain thereof is connected to said seventh MIS transistor, the gate of said sixth MIS transistor is connected to said seventh MIS transistor, and the drain thereof is connected to said eighth MIS transistor~~.

10. (currently amended) The semiconductor device according to claim 7, further comprising:

~~a ninth~~ an additional MIS transistor having a source-drain path between ~~the~~ an operating voltage supply point of said first memory cell and ~~the~~ a power line,

wherein said ~~ninth~~ additional MIS transistor is

controlled so as to be in the off state in a first state and to be in the on state in a second state, and

before said second state is changed to said first state, information of said first memory cell is stored into said second memory cell.

Claims 11-15 (cancelled)